Platform FPGA for Next Generation Performance

Xilinx HyperTransport Solution

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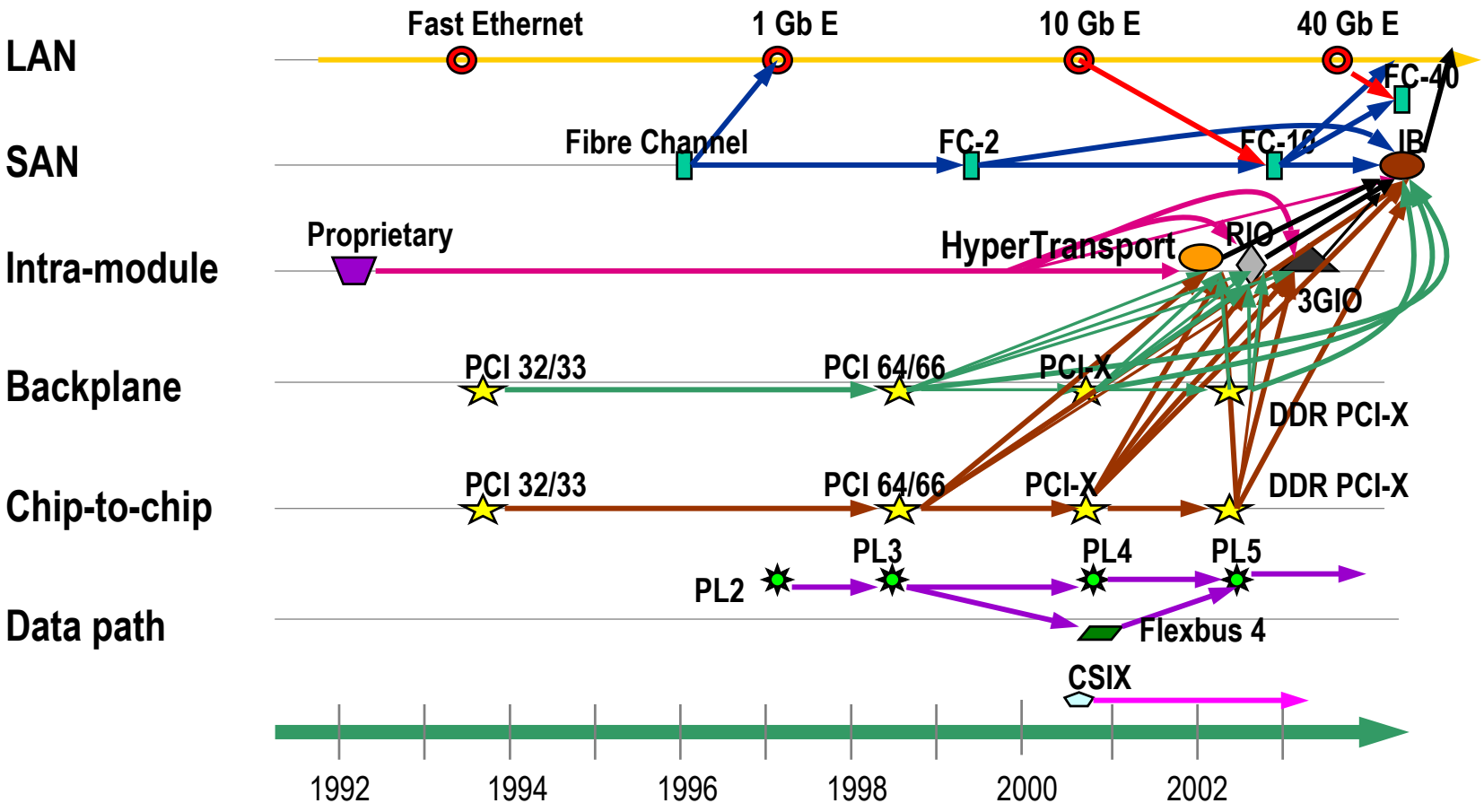
XILINX®
The Programmable Logic Company℠

HyperTransport™ CONSORTIUM

Explosion of New Connectivity Standards



A typical Terabit System will use two or more standards at a time!

Increased Usage of Future-Proof Programmable Solutions

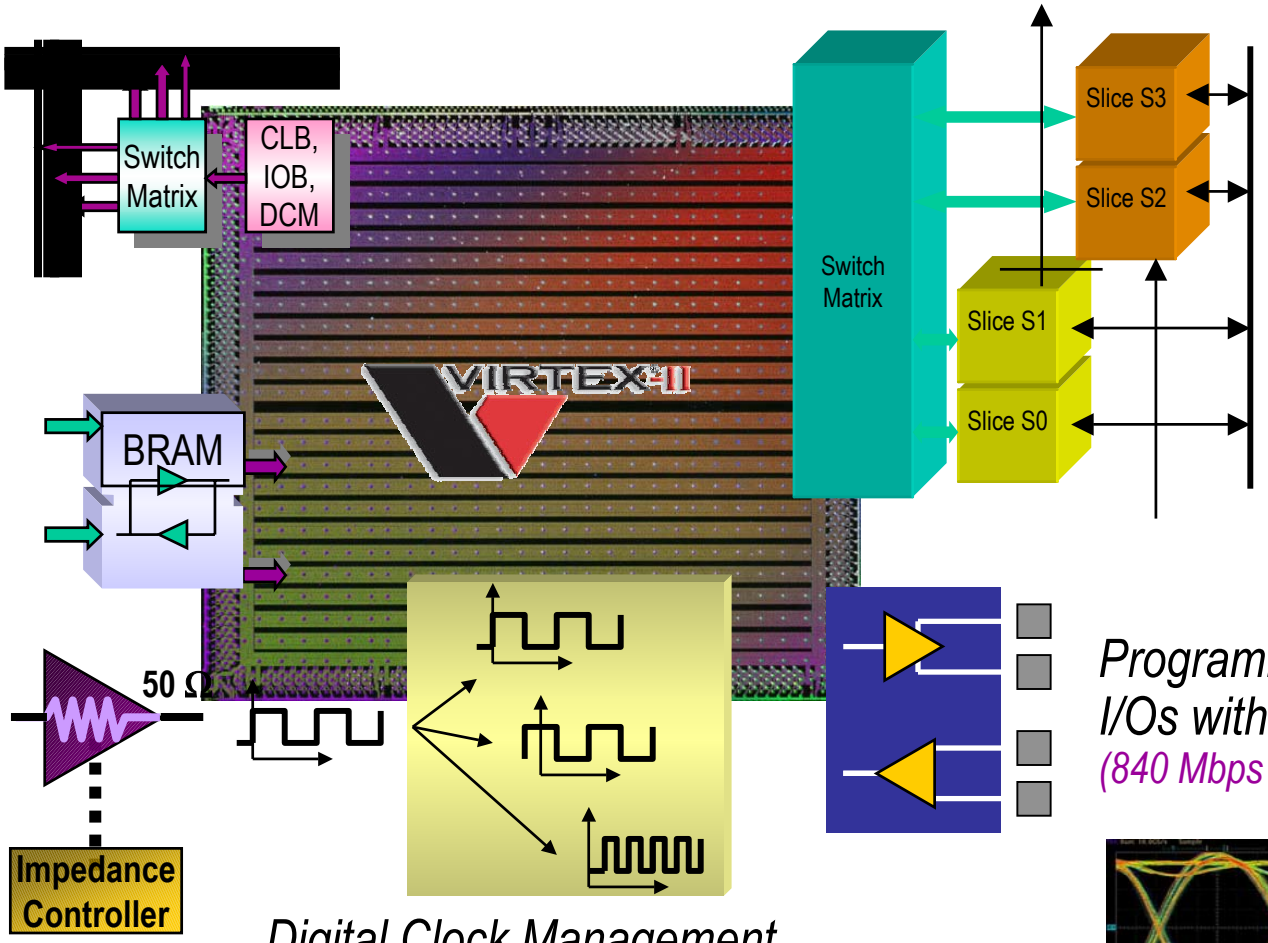
- Service providers and enterprises are looking to extend product life cycle and ROI
  - Field upgradeability allows product future-proofing
- Equipment manufacturers are looking to lower design risk by using "off-the-shelf" solutions
  - Allows adapting to evolving standards & changing specs
  - NPUs - customized functionality through C-code
  - FPGAs - customized functionality through HDL

Platform FPGA Value Propositions

Active interconnect™ Technology
Fast, predictable routing delays

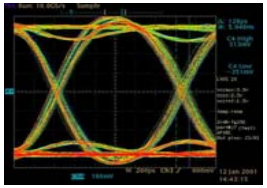
Abundances of On-chip RAM
Fast & efficient logic
Highest flexibility

On-chip termination
Improved signal integrity
Reduced lay-out complexity



Powerful CLB
>300 MHz Performance

Programmable I/Os with LVDS
(840 Mbps Eye)



Digital Clock Management
Precise frequency generation and phase control
Managing both on-chip & off-chip clock synchronization

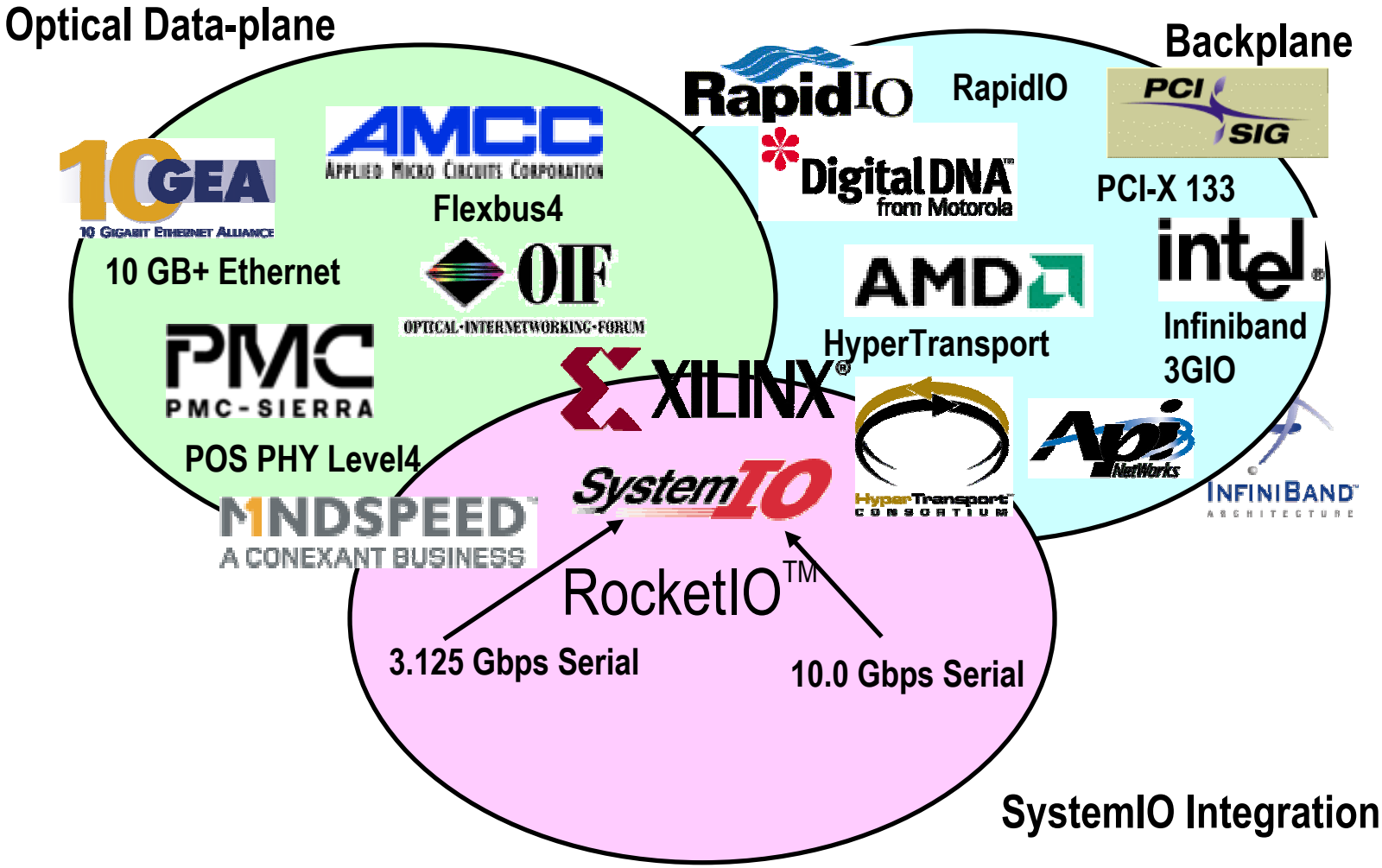
SystemIO Value Propositions

Reduced Risk and Design Flexibility

- Adapt to emerging standards
- Allow change to evolving std. specs
- Minimize time for “re-spins”
- Allow for future proofing

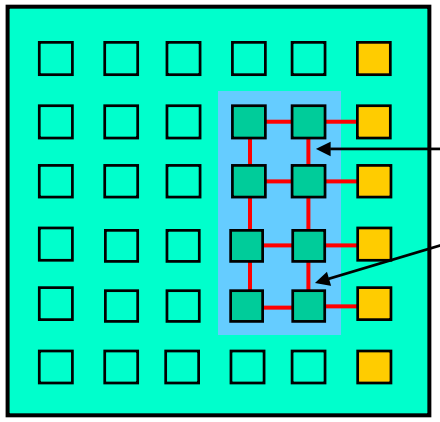
SystemIO Value Propositions

Standards Compliance & Proven Interoperability



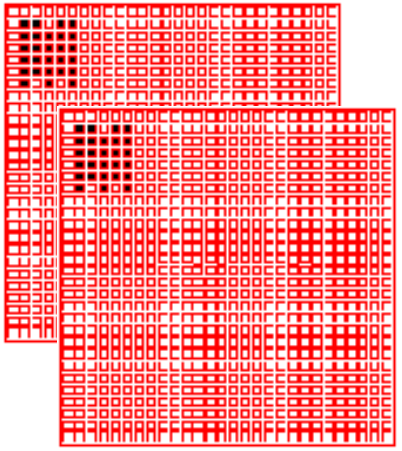
SystemIO Value Propositions

Improved Productivity



- SystemIO IP cores with pre-defined placement and routing
  - Improved predictability
  - Guaranteed performance

- SystemIO pre-verified IP cores advantages
  - Easy drop-in functionality
  - Improved Time-to-Market
  - Reduced Cost



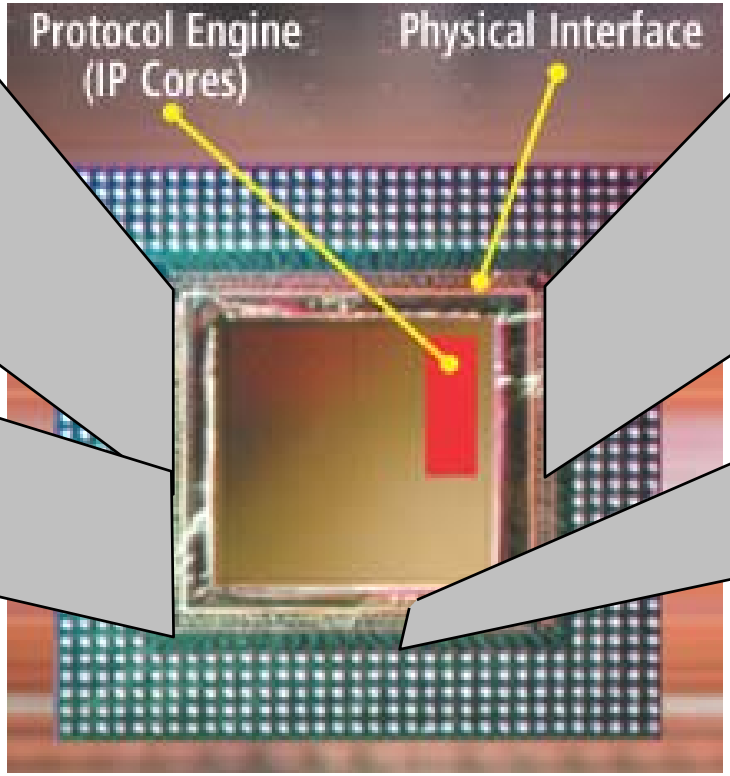
Platform FPGA SystemIO Solutions

System-Synchronous Parallel

- PCI 32,64-bit 33/66
- PCI-X 64-bit, 100

Source-Synchronous Parallel

- RapidIO™
- HyperTransport
- POS-PHY™ L3 & 4
- FlexBus 4™
- 1 & 10 Gigabit MACs
- XGMII
- CSIX-L1



Advanced Memory Interfaces

- ZBT SSRAM
- DDR SDRAM
- QDR SSRAM
- CAM

High-Speed Serial (Next Generation)

- Multi-Gigabit Backplanes
- Infiniband™
- Gigabit Ethernet PHY
- 10 Gigabit Ethernet - XAUI
- Fibre Channel

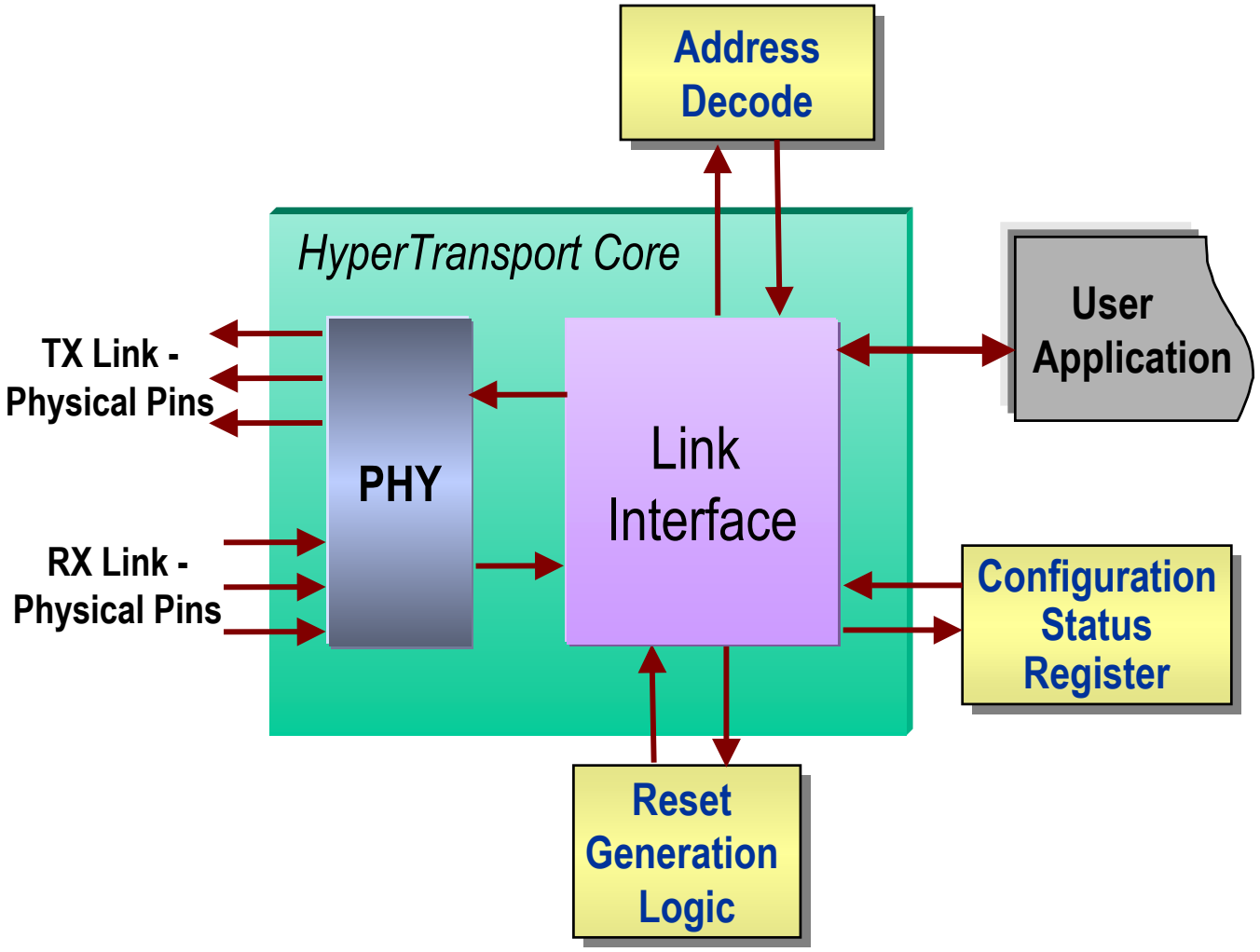
SystemIO = Protocol Engine (IP Cores) + Physical Interface(SelectI/O-Ultra™ technology)

Xilinx Collaborates with Industry Leaders

- Xilinx takes delivery of first HyperTransport FPGA Core
- Partnership with API NetWorks
  - Joint definition and engineering
  - Verification and optimization of core for Virtex-II
  - API FPGA switch demo based on 2V6000 device
- On SystemIO roadmap for release early '02
- Xilinx is a contributor level member in the HyperTransport Consortium

Xilinx HyperTransport Core

Block Diagram



Xilinx HyperTransport Solution

- Product Deliverables
  - Netlists
  - Constraints files
  - Instantiation templates: Verilog and VHDL
  - Datasheet
  - Sample testbench
- Product roadmap
  - Single-Ended Slave = available Q1'02
  - Tunnel and Host on SystemIO roadmap

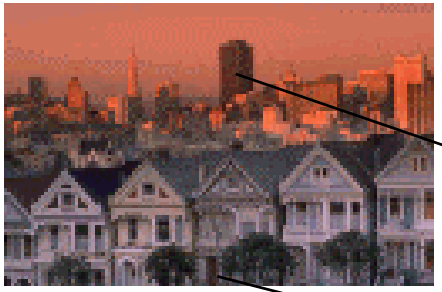
Only Xilinx SystemIO Provides Complete Connectivity Solution

From Chip-to-Chip to WAN

VIRTEX-II

LAN/MAN/WAN

- 10/100 Ethernet
- *1Gb Ethernet*
- ★ 10Gb Ethernet

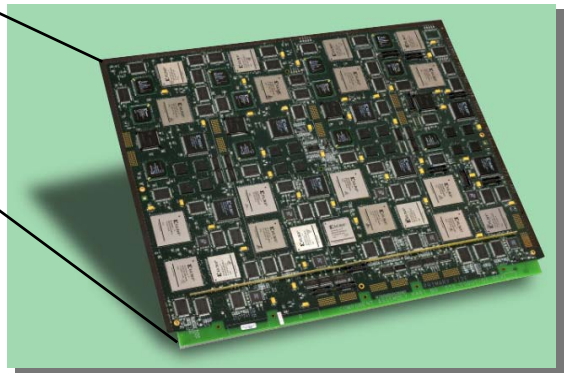


Board-to-Board

- ★ PCI 32/33
- ★ PCI 64/66
- ★ RapidIO
- ★ PCI-X 66 & 100
- *HyperTransport**

Chip-to-Chip

- ★ PCI 32/33
- ★ PCI 64/66
- ★ PCI-X 66 & 100
- ★ RapidIO
- ★ POS-PHY L3 & 4
- ★ Flexbus 4
- ★ CSIX
- *HyperTransport**



★ Semiconductor industry's first!

★ FPGA industry's first

* Available Q1/02